A2 cancelled

serves as one pixel 52, and a TFT 53 is provided for each pixel 52. Fig. 15 is a sectional view showing a construction of the TFT 53.

✓ Please rewrite the paragraph beginning on page 1, last line and ending on page 2, line 19 as follows:

(Amended) In the TFT 53, as shown in Fig. 15, a gate electrode 55 leading out of the gate line 50 is formed on a transparent substrate 54, and a gate insulating film 56 is formed in covering relation to the gate electrode 55. A semiconductor active film 57 made of amorphous silicon (a-Si) is formed on the gate insulating film 56 at a position above the gate electrode 55. A source electrode 59 leading out of the source line 51 and a drain electrode 60 are formed to extend over the semiconductor active film 57 through an ohmic contact layer 58 which is made of amorphous silicon (a-Si:n^+) containing an n-type impurity such as phosphorous, and then on the gate insulating film 56. A passivation film 61 is formed in covering relation to the TFT 53 made up of the source electrode 59, the drain electrode 60, the gate electrode 55, etc., and a contact hole 62 is formed in the passivation film 61 at a position above the drain electrode 60. Further, a pixel electrode 63 formed of a transparent conductive film, such as indium tin oxide (hereinafter referred to as ITO), is filled in the contact hole 62 for electrical connection to the drain electrode 60.

A3

✓ Please rewrite the paragraph beginning on page 2, line 20 and ending on page 3, line 9 as follows:

(Amended) Of the components of the TFT thus constructed, the gate insulating film located between the gate electrode and the semiconductor active film is the most important component that dominates electrical characteristics and reliability of the TFT. Also, the gate insulating film is an element that is responsible for the occurrence of surface defects. For an amorphous-silicon TFT using amorphous silicon as a material of the semiconductor active film, a redundant structure endurable against defects has been tried by employing a two-layered gate insulating film structure wherein gate insulating films are formed as two stacked layers using different materials and different methods. In one example of such a structure, the two stacked layers are a dense film of Ta_2O_5 formed by anode-oxidizing tantalum (Ta) of the gate electrode and a film of Si_3N_4 deposited by the plasma CVD.

A4